Signal Integrity- EMC Pro Tune Up

Pro Tune Up is a *(single day face to face session in the class room)* **Signal Integrity, Power Integrity, and EMI Control** class that gives students a solid explanation of proper high speed system design. Each student is expected to watch 2-3 hours of pre-class videos prior to the class. Post class homework includes Signal and Power Integrity simulations using a temporary HyperLynx license provided by Mentor Graphics. Between the pre-class videos and the post class simulation labs, PTU packs a 2-3 day class into a single day face to face session.

Pro Tune Up is based on a design methodology developed by a major telecommunications company which has been documented over multiple years and thousands of designs to produce "right the first time" results 99% of the time. "Right the first time" means the system works reliably at full speed. It has clearly defined design and manufacturing margins. It is also quiet enough to pass FCC & CISPR radiated emissions tests on the first try!

*Note*** I use Mentor HyperLynx for the labs, but this is not a tool class. It is a high speed system design methods class. As a design methods class it is equally applicable regardless of your tool chain.*

Target Audience: EE's, FPGA designers, CAD Layout Designers, and EMC guru's

Class Content :

Basic Signal Integrity including board layer stack-up specification, high speed routing topology, space, trace, termination practices, and return current control. Get this wrong and the system will reward you with a host of problems including False Clock, False Data, Negative Timing Margins, Clock Jitter, Excessive EMI as well as a host of Manufacturing and Reliability issues.

Power Integrity Power integrity depends upon stack-up, capacitor selection, placement, mounting technique, and quantity. Poor design can result in power impedance poles and inter plane resonances. Many of the mysterious SI and EMI issues can be traced directly to poor power system design.

Root causes and cures for EMI. The goal is to stop the EMI noise at the source. If EMI noise is eliminated at the source, you do not need to chase it around the board. Once you have controlled the noise source, the next issue is to avoid making an efficient antenna. You need to clearly understand the key reasons for EMI if you want to have any chance of repeatable success.

DDR3-4 Layout Issues Do you understand the four signal classes which make up a DDR3/4 memory interface? Do you know how to go from data sheet timing specifications to real world routing and topology constraints on the board? What is a "safe via?" Are routing distances pin to pin or die to die?

Differential Signaling What is the difference between Ethernet 10/100 Base T differential signaling and LVDS? With the huge noise margin available using LVDS devices, you can use almost any interconnect scheme. However there can be other nasty complications like Cross Talk and EMI if you do it incorrectly.

Giga Bit Serial - SERDES interface routing issues …PCI Express, 10GHz XAUI, etc.. We explain what is important and also debunk some of the popular myths about routing these types of interfaces. Do you understand how vias can cause a non-phase coherent channel?

The Analog / Digital Interface … i.e. Isolation vs. Communication There are many ways you can do this, but only one is easy to understand and produces repeatedly good results.

To Moat or Not to Moat Understanding the issues related to "quiet grounds." Signal ground vs. chassis ground..how do you connect them safely? Moating the ground plane usually causes EMI problems. Do you know why?

Connectors, Board to Board, Board to cable, etc. What are the SI, EMI, and Power issues. At the connector we still need to deal with physics.

Chip Level Package Issues What is critical about choosing FPGA pin out locations?

Basic Shielding & Filter Theory as it applies to Enclosures, Switching Power Supplies, and Renegade Chips

The High Speed System Design Process Performing a solid pre-layout design review with the correct personnel can raise you first time odds of success to at least 65%. Adding a solid post-layout design review can raise the odds of first time success 90%+ even the first time you go through the process.

Why should I attend this class?

Any Electrical Engineer, CAD Layout Designer, or Technical Manager who is tired of playing "Whack A Mole" would find this class extremely useful. Students who practice this methodology have regularly produced complex designs that work correctly and pass FCC/CISPR test on the first implementation. Right the first time design saves about $12,000 in out of pocket expenses and about 3 months of hardware design- debug time on the average project.

Questions??

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